FORM PTO-1390 (REV. 12-2001) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: 1406/53

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): 10/089424

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP00/09317	22 September 2000 (22.09.00)	30 September 1999 (30.09.99)

TITLE OF INVENTION: PCI BUS INTERFACE CIRCUIT

APPLICANT(S) FOR DO/EO/US: INFINEON TECHNOLOGIES, AG and FOEDLMEIER, Dieter

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (21) indicated below.
4. [X] The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [X] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. [X] is attached hereto.
   b. [ ] has been previously submitted under 35 U.S.C. 154(d)(4).
7. [X] Amendments to the claims of the International Aplication under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [X] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371 (c)(3)).
9. [X] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English lanugage translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 20 below concern document(s) or information included:

11. [X] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate c
13. [X] A FIRST preliminary amendment.
14. [ ] A SECOND or SUBSEQUENT preliminary amendm
15. [ ] A substitute specification.
16. [ ] A change of power of attorney and/or address letter.
17. [ ] A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
18. [ ] A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. [ ] A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. [X] Other items or information:

Copy of PCT Publication; copy of International Search Report; copy of International Preliminary Examination Report; copy of PCT/IB301; copy of PCT/IB/304; copy of PCT/IB/308

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I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Commissioner for Patents, Washington, D.C. 20231
Shay E. Dunn

U.S. APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
10/089424	PCT/EP00/09317	1406/53

JC10 Rec'd PCT/PTO 28 MAR 2002

21. [X] The following fees are submitted:	CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1)-(5)):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 890.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 0.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	12 - 20 =	0	x **$18.00**	$ 0.00	
Independent claims	1 - 3 =	0	x **$84.00**	$ 0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$280.00**	$ 0.00	
TOTAL OF ABOVE CALCULATIONS =				$ 0.00	
[ ] Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.			+	$ 0.00	
SUBTOTAL =				$ 890.00	
Processing fee of **$130.00** for furnishing the English translation later than [ ] 20 [ ] 30 months from the earliest claimed priority date (37 CFR 1.492(f)).				$ 0.00	
TOTAL NATIONAL FEE =				$ 890.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$ 0.00	
TOTAL FEES ENCLOSED =				$ 890.00	
				Amount to be refunded:	$
				charged:	$

a. [X] A check in the amount of $ 890.00 to cover the above fees is enclosed.

b. [ ] Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. [X] The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-0426 A duplicate copy of this sheet is enclosed.

d. [ ] Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137 (a) or (b)) must be filed and granted to restore the application to pending status.

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PATENT TRADEMARK OFFICE

Richard E Jenkins
SIGNATURE

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28,428
REGISTRATION NUMBER

10/089424

"Express Mail" mailing number ET871448655US
Date of Deposit 28 March 2002
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail to Addressee" service under 37 C.F.R 1 10 on the date indicated above and is addressed to the Commissioner for Patents, Washington, D C 20231
Shay E. Dunn

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Dieter Foedlmeier

Group Art Unit: Not Assigned

Serial No.: Not Assigned

Examiner: Not Assigned

Filed: Herewith

Docket No.: 1406/53

For: PCI BUS INTERFACE CIRCUIT

* *

PRELIMINARY AMENDMENT

Honorable Commissioner for Patents
BOX PCT
Washington, D.C. 20231

Dear Sir:

Kindly amend the subject application as follows:

IN THE SPECIFICATION:

Please insert the paragraph heading on page 1 of the English translation of the subject application, before line 5, as follows:

--Technical Field --.

Please insert the paragraph heading on page 1 of the English translation of the subject application, before line 9, as follows:

--Background Art --.

Please insert the paragraph heading on page 4 of the English translation of the subject application, before line 28, as follows:

--Summary of the Invention--.

Please insert the paragraph heading on page 7 of the English translation of the subject application, before line 5, as follows:

--Brief Description of the Drawings--.

Please insert the paragraph heading on page 7 of the English translation of the subject application, line 20, as follows:

--Detailed Description of the Invention--.

IN THE CLAIMS:

Please delete the paragraph heading on page 14 of the English translation of the subject application, line 1, and insert in place thereof the paragraph heading as follows:

--CLAIMS--

Please insert the paragraph heading on page 14 of the English translation of the subject application, before claim 1, the following:

-- What is claimed is: --.

Please amend claims 1-12 as follows:

1. (Amended) A PCI bus interface circuit for the voltage supply of a PCT plug-in card that can be connected to a PCI bus, having:

a first input for connection to a main voltage supply line of the PCI bus;

a second input for connection to an auxiliary voltage supply line of the PCI bus;

an output for outputting a supply voltage to the PCI plug-in card;

a first switching device for switching a main supply voltage that is present at the first input to the output if no auxiliary supply voltage V_{aux} is present at the second input;

a second switching device for switching an auxiliary supply voltage V_{aux} that is present at the second input to the output if no main supply voltage V_{cc} is present at the first input; and having

a third switching device, which, given the simultaneous presence of a main supply voltage V_{cc} at the first input and an auxiliary supply voltage V_{aux} at the second input, drives the second switching device for switching the auxiliary supply voltage V_{aux} through to the output.

2. (Amended) The interface circuit as claimed in claim 1, wherein the switching devices are semiconductor switches.

3. (Amended) The interface circuit as claimed in claim 1, wherein the switching devices are transistors each having a control terminal.

4. (Amended) The interface circuit as claimed in claim 1, wherein the switching devices are transistors, the third switching device being constructed complementarily with respect to the first and second switching devices.

5. (Amended) The interface circuit as claimed in claim 3, wherein the control terminal of the first transistor is connected to the second input and the control terminal of the second transistor is connected to the first input.

6. (Amended) The interface circuit as claimed in claim 3, wherein the control terminal of the third transistor is connected to the second input, the third transistor, when an auxiliary supply voltage is applied to the second input, turning on and connecting the control terminal of the second transistor to a specific voltage potential, with the results that the auxiliary supply voltage is switched through to the output.

7. (Amended) The interface circuit as claimed in claim 1, wherein respective current limiting resistors are connected upstream of the control terminals of the first and second transistors.

8. (Amended) The interface circuit as claimed in claim 1, wherein the switching point of the third switching device is adjustable by means of a voltage divider.

9. (Amended) The interface circuit as claimed in claim 1, wherein provision is made of a detection line, connected to the second input, for outputting the auxiliary supply voltage to a voltage detection device within the circuit situated on the plug-in card.

10. (Amended) The interface circuit as claimed in claim 1, wherein the switching devices have a small voltage drop in the turned-on state.

11. (Amended) The interface circuit as claimed in claim 10, wherein the switching devices have a voltage drop of less than 0.1 volt in the turned-on state.

12. (Amended) The interface circuit as claimed in claim 1, wherein the main supply voltage and the secondary supply voltage are in each case 3.1 volts to 3.5 volts.

REMARKS

The amendments to the specification as set forth above are intended to clarify and set apart the various sections of the subject application.

The amendments to the claims as set forth above are intended to remove all multiple dependent claims from the subject application and to more particularly point out and distinctly claim the subject invention.

Attached hereto is a marked-up version of the specification and claims 1-12, which illustrates all of the changes made to the specification and claims pursuant to 37 CFR §1.121. The attached page is captioned "**Version With Markings To Show Changes Made**". Deleted language is bracketed and added language is underlined.

The Commissioner is hereby authorized to charge any deficiencies or credit any overpayments in connection with the filing of this correspondence to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS & WILSON, P.A.

Date: 3-28-02 By: Richard E. Jenkins

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1406/53 REJ/lsg

25297
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Serial No.: Not yet assigned

Version With Markings To Show Changes Made

IN THE SPECIFICATION:

The paragraph heading has been inserted on page 1 of the English translation of the subject application, before line 5, as follows:

Technical Field

The paragraph heading has been inserted on page 1 of the English translation of the subject application, before line 9, as follows:

Background Art

The paragraph heading has been inserted on page 4 of the English translation of the subject application, before line 28, as follows:

Summary of the Invention

The paragraph heading has been inserted on page 7 of the English translation of the subject application, before line 5, as follows:

Brief Description of the Drawings

The paragraph heading has been inserted on page 7 of the English translation of the subject application, line 20, as follows:

Detailed Description of the Invention

IN THE CLAIMS:

The paragraph heading "Patent Claims" on page 14 of the English translation of the subject application has been deleted and the paragraph heading has been inserted in place thereof as follows:

CLAIMS

The paragraph heading has been inserted on page 14 of the English translation of the subject application, before claim 1, as follows:

What is claimed is:

1. (Amended) A PCI bus interface circuit for the voltage supply of a PCT plug-in card that can be connected to a PCI bus, having:

a first input [(2)] for connection to a main voltage supply line of the PCI bus;

a second input [(3)] for connection to an auxiliary voltage supply line of the PCI bus;

an output [(4)] for outputting a supply voltage to the PCI plug-in card;

a first switching device [(6)] for switching a main supply voltage that is present at the first input [(2)] to the output [(4)] if no auxiliary supply voltage V_{aux} is present at the second input [(3)];

a second switching device [(7)] for switching an auxiliary supply voltage V_{aux} that is present at the second input [(3)] to the output [(4)] if no main supply voltage V_{cc} is present at the first input [(2)] ; and having

a third switching device [(20)], which, given the simultaneous presence of a main supply voltage V_{cc} at the first input [(2)] and an auxiliary supply voltage V_{aux} at the second input [(3)], drives the second switching device [(7)] for switching the auxiliary supply voltage V_{aux} through to the output [(4)].

2. (Amended) The interface circuit as claimed in claim 1, wherein the switching devices [(6, 7, 20)] are semiconductor switches.

3. (Amended) The interface circuit as claimed in claim 1 [or 2], wherein the switching devices [(6, 7, 20)] are transistors each having a control terminal [(11, 9, 21)].

4. (Amended) The interface circuit as claimed in [one of the preceding claims] claim 1, wherein the switching devices [(6, 7, 20)] are transistors, the third switching device [(20)] being constructed complementarily with respect to the first and second switching devices [(6, 7)].

5. (Amended) The interface circuit as claimed in [one of the preceding claims] claim 3, wherein the control terminal [(11)] of the first transistor [(6)] is connected to the second input [(3)] and the control terminal [(9)] of the second transistor [(7)] is connected to the first input [(2)].

6. (Amended) The interface circuit as claimed in [one of the preceding claims] claim 3, wherein the control terminal [(21)] of the third transistor [(20)] is connected to the second input [(3)], the third transistor [(20)], when an auxiliary supply voltage is applied to the second input [(3)], turning on and connecting the control terminal [(9)] of the second transistor [(7)] to a specific voltage potential, with the results that the auxiliary supply voltage is switched through to the output [(4)].

7. (Amended) The interface circuit as claimed in [one of the preceding claims] claim 1, wherein respective current limiting resistors [(28, 27)] are connected upstream of the control terminals of the first and second transistors [(6, 7)].

8. (Amended) The interface circuit as claimed in [one of the preceding claims] claim 1, wherein the switching point of the third switching device [(20)] is adjustable by means of a voltage divider [(19, 33)].

9. (Amended) The interface circuit as claimed in [one of the preceding claims] claim 1, wherein provision is made of a detection line [(17)], connected to the second input [(3)], for outputting the auxiliary supply voltage to a voltage detection device within the circuit situated on the plug-in card.

10. (Amended) The interface circuit as claimed in [one of the preceding claims] claim 1, wherein the switching devices [(6, 7, 20)] have a small voltage drop in the turned-on state.

11. (Amended) The interface circuit as claimed in [one of the preceding claims] claim 10, wherein the switching devices [(6, 7, 20)] have a voltage drop of less than 0.1 volt in the turned-on state.

12. (Amended) The interface circuit as claimed in [one of the preceding claims] claim 1, wherein the main supply voltage and the secondary supply voltage are in each case 3.1 volts to 3.5 volts.

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Description

PCI bus interface circuit

The invention relates to a PCI bus interface circuit for the voltage supply of a plug-in card circuit that can be connected to a PCI bus.

The PCI bus system is used primarily in the PC sector. In this case, the majority of PCs have both PCI slots and, for reasons of compatibility, ISA slots.

Figure 1 shows the basic construction of a PCI bus system. Plug-in cards K1, K2, K3 are connected to the main circuit board or motherboard of the computer via the PCI bus. For this purpose, the plug-in cards K1, K2, K3 are inserted into the PCI slots. The power supply of the plug-in cards K1, K2, K3 is likewise effected via the PCI bus.

Older PCI plug-in cards K1, K2, K3 do not carry out power supply management or power management and are only supplied with a main supply voltage V_{CC}. Such PCI plug-in cards are increasingly being replaced by plug-in cards which carry out power supply management in order to save energy. For this purpose, the PCI plug-in cards have to be supplied with a secondary supply voltage or auxiliary supply voltage V_{aux} via the PCI bus. The secondary supply voltage, having a small loading capability, supplies the PCI plug-in cards K1, K2, K3 in a standby mode or is used for the start-up of the computer by the PCI plug-in cards, the PCI plug-in cards being supplied with the main supply voltage V_{CC} after start-up has been effected.

Since not all PCI bus systems are provided with a secondary voltage supply line for supplying the PCI plug-in cards with a secondary or auxiliary supply

voltage V_{aux}, an interface circuit is provided on the PCI plug-in cards. The interface circuit ensures that the PCI plug-in cards are supplied with the main supply voltage V_{CC} if no auxiliary supply voltage V_{aux} is present. Conversely, when an auxiliary supply voltage V_{aux} is present on the PCI bus, the PCI plug-in card K receives said auxiliary supply voltage for carrying out the power supply management.

Figure 2 shows an interface circuit according to the prior art.

The interface circuit has two signal inputs E1, E2. The main supply voltage V_{CC} is applied to the input E1, while the input E2 is connected to the auxiliary voltage supply line of the PCI bus. Furthermore, the interface circuit shown in figure 2 has an output A for outputting a supply voltage to a circuit situated on the PCI plug-in card. The circuit situated on the plug-in card detects the presence of an auxiliary supply voltage V_{aux}, applied to the input E2, via a detection line D. If no auxiliary supply voltage V_{aux} is present at the input E2, the detection device of the circuit situated on the PCI plug-in card is pulled to ground via a pull-down resistor R. As a result, the detection device receives a logically unambiguous signal indicating that no auxiliary supply voltage is present.

The interface circuit according to the prior art, as is shown in figure 2, contains two switching devices S1, S2, which are formed by two complementary transistors in the example shown in figure 2. In this case, the transistor S1 is an N-channel FET, while the transistor S2 is a P-channel FET. The control terminals of the two transistors S1, S2 are connected to the input E2. If the auxiliary supply voltage V_{aux} is present at the input E2, the FET transistor S1 is turned on or activated, and, at the same time, the FET transistor S2

is turned off or deactivated. As a result, the auxiliary supply voltage for the PCI plug-in card is present at the output A. At the same time, the auxiliary supply voltage V_{aux} present at the input E2 is detected by a voltage detection device, present on the PCI plug-in card, via the signal output D of the interface circuit.

If the main supply voltage V_{CC} is present at the input E1 and if, at the same time, no auxiliary supply voltage V_{aux} is applied to the input E2, the FET transistor S1 turns off and the complementary FET transistor S2 is turned on, with the result that the plug-in card circuit is supplied with the main supply voltage V_{CC} via the output A of the interface circuit.

If the main supply voltage V_{CC} is present at the input E1 and, at the same time, the auxiliary supply voltage V_{aux} is present at the input E2, the FET transistor S1 is turned on and the FET transistor S2 is turned off, with the result that the auxiliary supply voltage V_{aux} is present at the output A of the interface circuit in this case.

The table below shows the various operating cases for the interface circuit according to the prior art, as is shown in figure 2.

Table 1
(Prior art)

Operating case	**E1**	**E2**	**S1**	**S2**	**Δ**
B1	0	0	off	on	0
B2	V_{CC}	0	off	on	V_{CC}
B3	0	V_{aux}	on	off	V_{aux}
B4	V_{CC}	V_{aux}	on	off	V_{aux}

The interface circuit according to the prior art as shown in figure 2 has the disadvantage, however, that it does not ensure a reliable voltage supply of the PCI plug-in card circuit in every operating case. In PCI bus systems, the main supply voltage V_{CC} and also the auxiliary supply voltage V_{aux} are 3.3 volts in each case. The supply voltage of the circuit situated on the plug-in card should never be below 3 volts. Therefore, it must be ensured that, at the output A of the interface circuit, given the presence of a supply voltage on the PCI bus, likewise at least an output voltage of 3 volts is output to the PCI plug-in card K.

In operating case B3 (see table), the auxiliary supply voltage V_{aux} is present at the input E2, while no main supply voltage V_{CC} is present at the input E1. In this case, the FET transistor S1 is turned on and the FET transistor S2 turns off. The FET transistor S1 acts like a forward-biased diode across which a diode forward voltage of about 0.7 volt is dropped. Given an auxiliary supply voltage of 3.3 volts, only a supply voltage of about 2.6 volts thus passes to the output A of the interface circuit according to the prior art. In other words, this supply voltage is clearly below the required 3 volts which are necessary for the reliable voltage supply of the circuit on the PCI plug-in card.

The object of the present invention, therefore, is to provide a PCI bus interface circuit which ensures, in every operating case, a reliable voltage supply of the PCI plug-in card circuits connected to the PCI bus.

This object is achieved according to the invention by means of a PCI bus interface circuit with the features specified in patent claim 1.

Further advantageous refinements of the PCI bus interface circuit according to the invention are specified in the subclaims.

The invention provides a PCI bus interface circuit for the voltage supply of a PCI plug-in card that can be connected to the PCI bus, having:
a first input for connection to a main voltage supply line of the PCI bus;
a second input for connection to an auxiliary voltage supply line of the PCI bus;
an output for outputting a supply voltage to the PCI plug-in card;
a first switching device for switching a main supply voltage that is present at the first input to the output
if no auxiliary supply voltage is present at the second input;
a second switching device for switching an auxiliary supply voltage that is present at the second input to the output
if no main supply voltage is present at the first input; and having
a third switching device, which, given the simultaneous presence of a main supply voltage at the first input and an auxiliary supply voltage at the second input, drives the second switching device for switching the auxiliary supply voltage through to the output.

In a preferred development of the interface circuit according to the invention, the switching devices are semiconductor switching devices.

In a preferred further embodiment of the interface circuit according to the invention, the switching devices are transistors each having a control terminal.

The third switching device is preferably complementary to the first and second switching devices.

In a further preferred development of the interface circuit according to the invention, the control terminal of the first transistor is connected to the second input and the control terminal of the second transistor is connected to the first input.

In accordance with a preferred development, the control terminal of the third transistor is connected to the second input, the third transistor, given the presence of an auxiliary supply voltage at the second input, being turned on and connecting the control terminal of the second transistor to a predetermined voltage potential, in order that the second transistor switches the auxiliary supply voltage through to the output.

Respective current limiting resistors are preferably connected upstream of the control terminals of the transistors.

In a further preferred development, the switching point of the third switching device is adjustable by means of a voltage divider.

In a further preferred development, provision is made of a detection line, connected to the second input, for the detection of the auxiliary supply voltage by a voltage detection device on the PCI plug-in card.

The switching devices preferably have a small voltage drop in the turned-on state.

In a preferred embodiment, the switching devices have a voltage drop of less than 0.1 volt in the turned-on state.

Preferably, the main supply voltage and also the auxiliary supply voltage are nominally 3.3 volts in each case.

Furthermore, a preferred embodiment of the interface circuit according to the invention is described with reference to the accompanying drawings in order to elucidate features that are essential to the invention.

In the figures:

Figure 1 shows a block diagram for illustrating a conventional PCI bus system;
Figure 2 shows a PCI bus interface circuit according to the prior art;
Figure 3 shows a PCI bus interface circuit according to the invention;
Figure 4 shows a preferred embodiment of the PCI bus interface circuit according to the invention.

As can be seen from figure 3, the PCI bus interface circuit 1 according to the invention has a first input 2 for connection to a main voltage supply line of a PCI bus and also a second input 3 for connection to an auxiliary voltage supply line of the PCI bus. Furthermore, provision is made of an output 4 for outputting a supply voltage to a PCI plug-in card. Moreover, the interface circuit according to the invention has an output terminal 5 for the connection of a voltage detection device on the PCI plug-in card, which can detect an auxiliary supply voltage V_{aux} that is present at the input terminal 3.

The interface circuit contains a first controllable switching device 6 for switching the main supply voltage V_{CC} that is present at the first input 2 through to the output 4. Furthermore, the interface circuit contains a second switching device 7 for switching an

auxiliary supply voltage that is present at the second input 3 through to the output 4. The input 2 is connected via an internal line 8 to a control terminal 9 of the second switching device 7, while the second input 3 is connected via an internal line 10 to a control terminal 11 of the first switching device 6. In a manner dependent on the signal present at the control terminal 11, the first switching device 6 switches the main supply voltage V_{CC} that is present at the input 2 via lines 12, 13 onto a line 14, which is connected to the output 4. In a manner dependent on the signal present at the control terminal 9, the second switching device 7 switches, via a line 15, an auxiliary supply voltage V_{aux} that is present at the second input 3 onto the line 14 for outputting via the output terminal 4.

The internal line 10 connected to the input 3 has a junction node 16, at which a line 17 is routed to the output terminal 5 and at which, moreover, a line 18 branches off, which is grounded via a resistor 19. A third switching device 20 with a control terminal 21 is controlled via a control line 22 connected to a branch-off node 23 on the line 18. The third switching device 20 is connected to the line 8 via a line 24 at a junction node 25. Furthermore, the third switching device 20 is grounded via a line 26.

The first switching device 6 switches the main supply voltage that is present at the first input 2 to the output 4 if no auxiliary supply voltage V_{aux} is present at the second input 3. If an auxiliary supply voltage V_{aux} is not present, the voltage potential at the node 16 is pulled to ground via the pull-down resistor 19 and drives the first switching device 6 via the line 10 and the control terminal 11 in such a way that the main supply voltage V_{CC} present on the line 12 is switched through onto the line 13 and thus passes via the line 14 to the voltage supply output 4.

The second switching device 7 switches an auxiliary supply voltage that is present at the second input 3 to the output 4 if no main supply voltage V_{CC} is present at the first input 2. In the case of a low-level main supply voltage V_{CC}, the second switching device 7 is driven via the line 8 and the control terminal 9 in such a way that it switches the auxiliary supply voltage V_{aux} that is present on the line 15 through to the line 14 for outputting via the output 4.

Given the simultaneous presence of a main supply voltage V_{CC} at the first input 2 and an auxiliary supply voltage V_{aux} at the second input 3, the third switching device 20 is driven via the lines 18, 22 in such a way that it through-connects the node 25 to ground via the lines 24, 26. As a result of the low potential present at the node 25, the second switching device 7 is driven for switching the auxiliary supply voltage present on the line 15 through to the line 14, with the result that the auxiliary supply voltage V_{aux} is present at the output 4 of the interface circuit. At the same time, the high potential present at the control terminal 11 of the first switching device 6 turns the switching device 6 off.

The table below shows the various operating cases of the interface circuit according to the invention.

Table 2

Operating case	**E1**	**E2**	**S6**	**S7**	**S20**	**Δ**
B1	0	0	on	on	off	0
B2	V_{CC}	0	on	off	on	V_{CC}
B3	0	V_{aux}	off	on	on	V_{aux}
B4	V_{CC}	V_{aux}	off	on	on	V_{aux}

Figure 4 shows a preferred embodiment of the interface circuit according to the invention. In this case, identical reference symbols specify structural parts corresponding to those in figure 3.

The switching devices 6, 7, 20 are preferably designed as semiconductor switches. In this case, the semiconductor switches are preferably transistors which are controlled by a control terminal 9, 11, 21.

As can be seen from figure 4, the third switching device, as NPN transistor 20, is complementary to the PNP transistors 6, 9 which form the first and second switching devices. As illustrated in figure 4, the semiconductor switches 6, 7, 20 may be constructed as bipolar transistors or, as an alternative, as field-effect transistors. Respective current limiting resistors 27, 28 are connected upstream of the control terminals 9, 11 of the two PNP transistors 7, 6. A further resistor 31 is connected to a branch-off node 29 via a line 30, said further resistor being grounded via a line 32. The resistor 31 serves as pull-down resistor which pulls the control terminal 9 of the transistor 7 to ground in the absence of a main supply voltage V_{CC} at the first input 2, with the result that the transistor 7 reliably switches an auxiliary voltage present at the second input 3 through to the output 4.

A resistor 33, which is preferably connected into the line 18, forms, together with the resistor 19, a voltage divider by means of which the switching point of the third switching device 20 is adjustable. An additional resistor 34 connected into the line 26 likewise serves for current limiting.

In the turned-on state, the semiconductor switching devices 6, 7, 20 operate in the low-impedance region, in which a voltage drop of less than 0.1 volt occurs.

The low-impedance region is the saturation region in bipolar transistors, while the low-impedance region is the triode region in field-effect transistors. Thus, a voltage drop of less than 0.1 volt is produced between the lines 12, 13 when the first switching device 6 turns on, and a voltage drop likewise of less than 0.1 volt is produced between the lines 15 and 14 when the switching device 7 turns on. If the auxiliary supply voltage at the second input 3 is nominally 3.3 volts, which may fluctuate in a range from 3.1 volts to 3.5 volts, in operating cases B3, B4 (see table 2) a supply voltage of about nominally 3.2 volts reaches the output, which supply voltage is at least 3 volts and thus satisfies the required 3 volts for the reliable voltage supply of the circuit situated on the plug-in card. Given the absence of an auxiliary supply voltage and presence of a main supply voltage at the first input 2 of the interface circuit (operating case B2 in table 2), the switching device 6 is turned on, a voltage drop of 0.1 volt being produced, with the result that a main supply voltage likewise of about 3.2 volts is present at the output 4. Thus, in every operating case, the interface circuit according to the invention ensures a reliable voltage supply of the circuit situated on the PCI plug-in card via the output 4.

A further advantage of the interface circuit according to the invention is that reliable decoupling of the auxiliary supply voltage V_{aux} and the main supply voltage is ensured. When a main supply voltage V_{CC} occurs at the first input 2 of the interface circuit and, at the same time, no auxiliary supply voltage V_{aux} is present at the second input 3 (see table 2, operating case B2), a high potential is present at the potential node 25, with the result that a reverse-biased PN junction is present between the control terminal 9 and the line 15, and prevents the main

supply voltage present at the input 2 from coupling onto the line 15. This ensures that there is no feedback of main supply voltage V_{CC} via the line 15, the line 10, the node 16 and via the line 17 to the output terminal 5. As a result, an auxiliary supply voltage that is not actually present cannot be erroneously detected by the voltage detection device situated on the plug-in card.

The resistors 19, 33 together form a voltage divider for setting the switching point of the switching device 20. The resistors 19, 33 are preferably variable resistors, so that the switching point of the switching device 20 is likewise adjustable.

In an alternative embodiment, the switching devices 7, 12, 20 may be constructed using discrete components, such as relay circuits for example.

List of reference symbols

1	PCI bus interface circuit
2	First input
3	Second input
4	Output
5	Detection output
6	First switching device
7	Second switching device
8	Line
9	Control terminal
10	Line
11	Control terminal
12	Line
13	Line
14	Line
15	Line
16	Node
17	Line
18	Line
19	Resistor
20	Third switching device
21	Control terminal
22	Line
23	Node
24	Line
25	Node
26	Line
27	Current limiting resistor
28	Current limiting resistor
29	Node
30	Line
31	Resistor
32	Line
33	Resistor
34	Resistor

Patent claims

1. A PCI bus interface circuit for the voltage supply of a PCI plug-in card that can be connected to a PCI bus, having:
a first input (2) for connection to a main voltage supply line of the PCI bus;
a second input (3) for connection to an auxiliary voltage supply line of the PCI bus;
an output (4) for outputting a supply voltage to the PCI plug-in card;
a first switching device (6) for switching a main supply voltage that is present at the first input (2) to the output (4) if no auxiliary supply voltage V_{aux} is present at the second input (3);
a second switching device (7) for switching an auxiliary supply voltage V_{aux} that is present at the second input (3) to the output (4) if no main supply voltage V_{CC} is present at the first input (2); and having
a third switching device (20), which, given the simultaneous presence of a main supply voltage V_{CC} at the first input (2) and an auxiliary supply voltage V_{aux} at the second input (3), drives the second switching device (7) for switching the auxiliary supply voltage V_{aux} through to the output (4).

2. The interface circuit as claimed in claim 1, wherein
the switching devices (6, 7, 20) are semiconductor switches.

3. The interface circuit as claimed in claim 1 or 2, wherein
the switching devices (6, 7, 20) are transistors each having a control terminal (11, 9, 21).

4. The interface circuit as claimed in one of the preceding claims,
wherein
the switching devices (6, 7, 20) are transistors, the third switching device (20) being constructed complementarily with respect to the first and second switching devices (6, 7).

5. The interface circuit as claimed in one of the preceding claims,
wherein
the control terminal (11) of the first transistor (6) is connected to the second input (3) and the control terminal (9) of the second transistor (7) is connected to the first input (2).

6. The interface circuit as claimed in one of the preceding claims,
wherein
the control terminal (21) of the third transistor (20) is connected to the second input (3), the third transistor (20), when an auxiliary supply voltage is applied to the second input (3), turning on and connecting the control terminal (9) of the second transistor (7) to a specific voltage potential, with the result that the auxiliary supply voltage is switched through to the output (4).

7. The interface circuit as claimed in one of the preceding claims,
wherein
respective current limiting resistors (28, 27) are connected upstream of the control terminals of the first and second transistors (6, 7).

8. The interface circuit as claimed in one of the preceding claims,

wherein
the switching point of the third switching device (20) is adjustable by means of a voltage divider (19, 33).

9. The interface circuit as claimed in one of the preceding claims,
wherein
provision is made of a detection line (17), connected to the second input (3), for outputting the auxiliary supply voltage to a voltage detection device within the circuit situated on the plug-in card.

10. The interface circuit as claimed in one of the preceding claims,
wherein
the switching devices (6, 7, 20) have a small voltage drop in the turned-on state.

11. The interface circuit as claimed in one of the preceding claims,
wherein
the switching devices (6, 7, 20) have a voltage drop of less than 0.1 volt in the turned-on state.

12. The interface circuit as claimed in one of the preceding claims,
wherein
the main supply voltage and the secondary supply voltage are in each case 3.1 volts to 3.5 volts.

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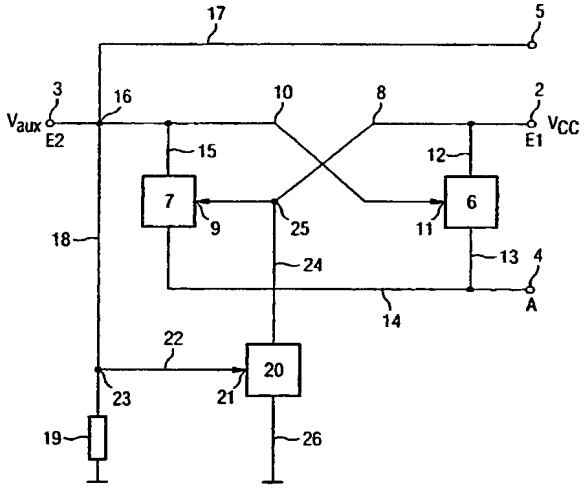
— *Mit internationalem Recherchenbericht.*
— *Vor Ablauf der für Änderungen der Ansprüche geltenden Frist; Veröffentlichung wird wiederholt, falls Änderungen eintreffen.*

[Fortsetzung auf der nächsten Seite]

(54) Title: PCI BUS INTERFACE CIRCUIT

(54) Bezeichnung: PCI-BUS-SCHNITTSTELLENSCHALTUNG



(57) Abstract: The invention relates to a PCI bus interface circuit for supplying power to a PCI plug-in card that is connected to a PCI bus. The inventive PCI bus interface circuit comprises a first input (2) for connection to a main voltage supply line of the PCI bus and a second input (3) for connection to an auxiliary voltage supply line of the PCI bus. The circuit further comprises an output (4) for delivering a supply voltage to the PCI plug-in card and a first switching means (6) for switching a main supply voltage supplied at the first input (2) to the output (4) when no auxiliary supply voltage V_{aux} is supplied at the second output (3). A second switching means (7) switches an auxiliary supply voltage V_{aux} supplied at the second input (3) to the output (4) when no main supply voltage V_{CC} is supplied at the first input (2). The inventive circuit further comprises a third switching means (20) that switches the second switching means (7) to switch the auxiliary supply voltage to the output (4) when a main supply voltage is supplied at the first input (2) while an auxiliary supply voltage is simultaneously supplied at the second input (3).

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FIG 1

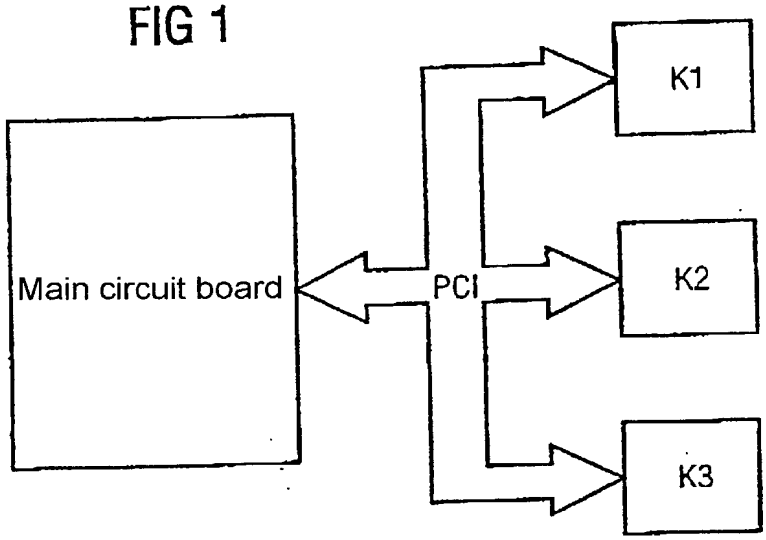

FIG 2

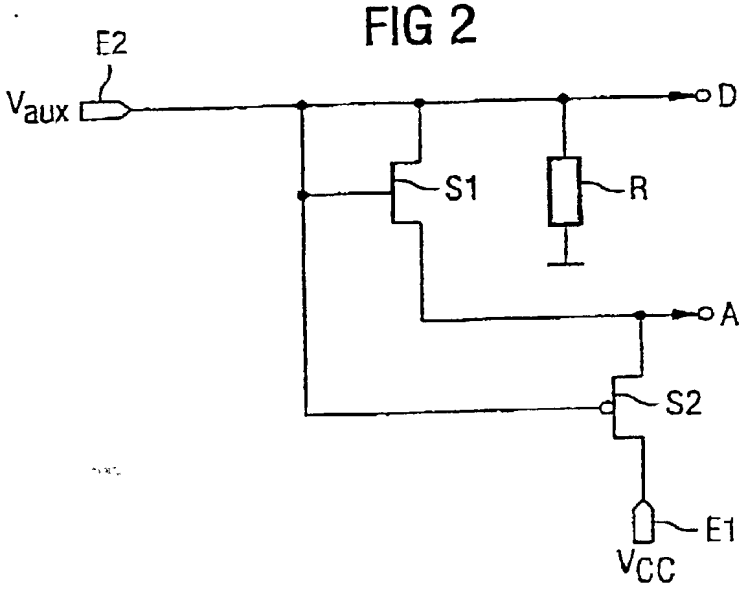

FIG 3

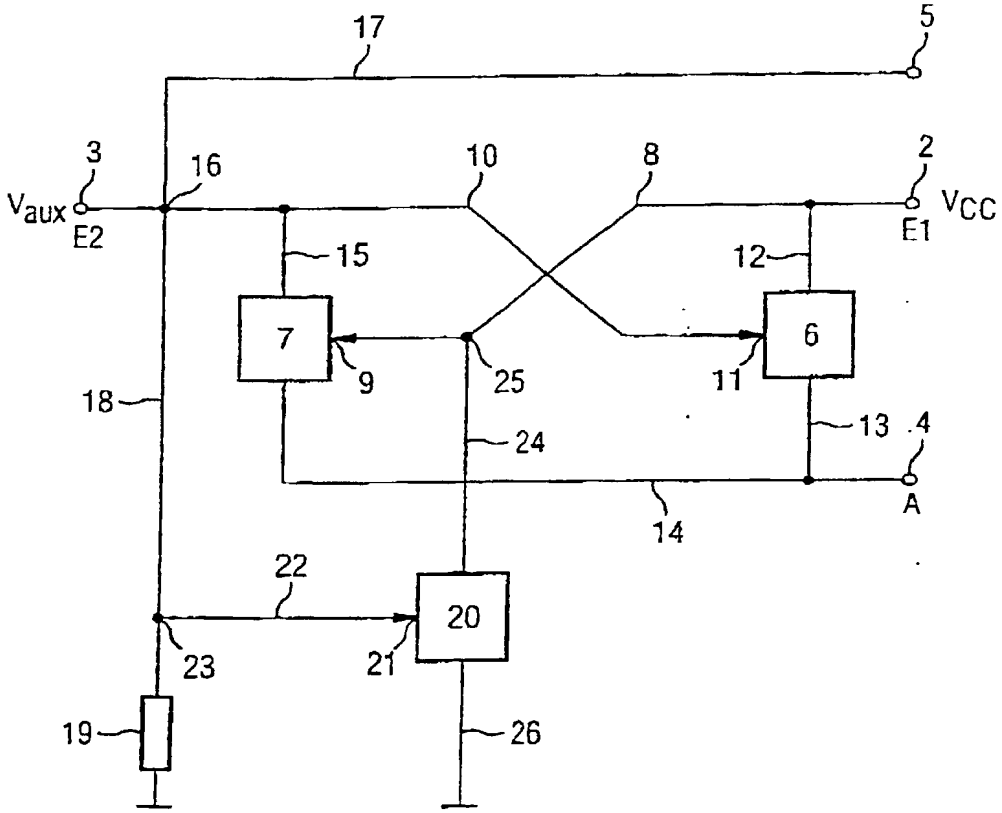
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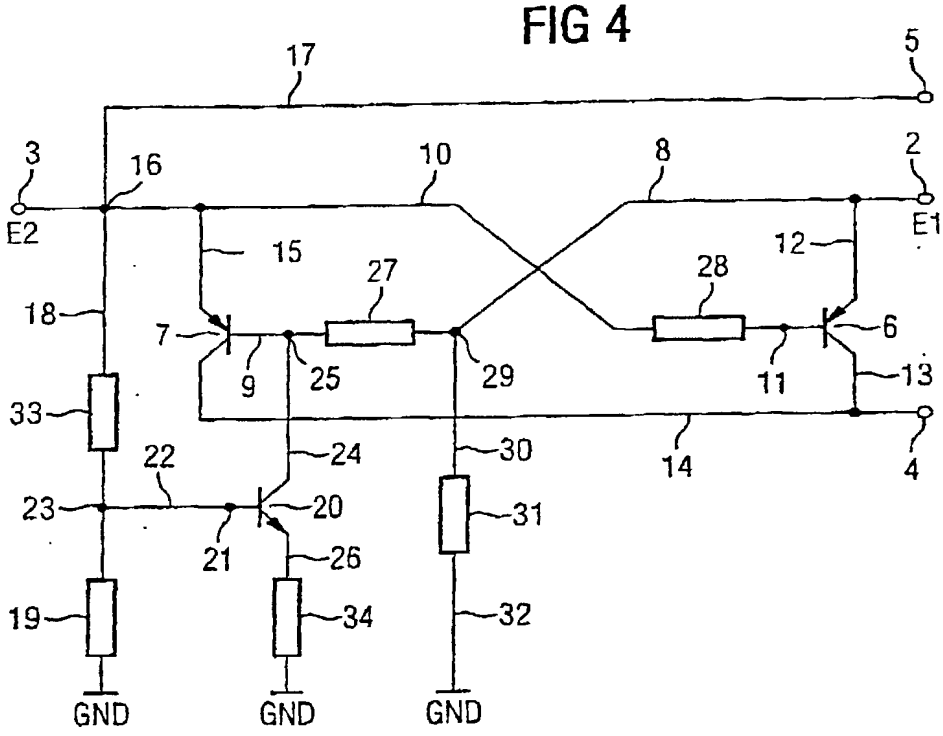
FIG 4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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☐ Declaration Submitted with Initial Filing OR ☒ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	1406/53
First Named Inventor	Foedlmeier, Dieter
COMPLETE IF KNOWN	
Application Number	10 / 089,424
Filing Date	March 28, 2002
Art Unit	
Examiner Name	

As the below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below next to my name

I believe I am the original and first inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

PCI BUS INTERFACE CIRCUIT

(Title of the Invention)

the specification of which

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY) 03/28/2002 as United States Application Number or PCT International Application Number 10/089,424 and was amended on (MM/DD/YYYY) _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	Certified Copy Attached? NO
199 47 017.0	Germany	09/30/1999	☐	☐	☒
PCT/EP00/09317	WIPO	09/22/2000	☐	☐	☒
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

PTO/SB/01 (10-01)
Approved for use through 10/31/2002 OMB 0651-0032
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

NAME OF SOLE OR FIRST INVENTOR : [ ] A petition has been filed for this unsigned inventor

Given Name (first and middle [if any]) 1-00 Dieter | Family Name or Surname Foedlmeier

Inventor's Signature Dieter Fällmeier | Date 27.6.2002

Residence: City Altdorf | State | Country DE | Citizenship DE DEK

Mailing Address Pfettrachweg 1

City Altdorf | State | ZIP 84032 | Country Germany

NAME OF SECOND INVENTOR: [ ] A petition has been filed for this unsigned inventor

Given Name (first and middle [if any]) | Family Name or Surname

Inventor's Signature | Date

Residence: City | State | Country DE | Citizenship

Mailing Address

City | State | ZIP | Country

[ ] Additional inventors are being named on the ____supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.